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AUTOMATION OF PRE-CAP VISUAL INSPECTION FOR INTEGRATED CIRCUITS

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18. SUPPLEMENTARY NOTES This project has been accomplished as part of the U.S. Army's Materials Testing Technology Program, which has for its objective the timely establishment of testing techniques, procedures, and prototype equipment (in mechanical, chemical, and non-destructive testing) to ensure efficient inspection methods for material/materiel procured and maintained by DARCOM.

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The feasibility of an automatic inspection system which can perform a 100% internal visual inspection of integrated circuits (ICs) during production was investigated. Columbia Research Corporation (CRC) reviewed technical approaches and the feasibility of applying them to production. They also surveyed the companies currently developing automated IC inspection systems and found that no commercial contractor has installed equipment for routine inspection on a production basis. This project was terminated because the necessary equipment is still undergoing design and evaluation.

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SUMMARY

This report presents the findings and conclusions of an investigation conducted by Columbia Research Corporation (CRC) under the direction of U.S. Army Armament Research and Development Command, DRDAR-QAT-1, Dover, New Jersey regarding the availability of an automated test system to perform pre-cap visual inspection of integrated circuits (ICs). Specifically the object was to collect, review, and evaluate information for developing a method to automatically perform the internal visual inspection of ICs per Test Method 2010.4 of MIL-STD-883B, incorporating the accept or reject criteria at production rates. Columbia Research Corporation has surveyed commercial IC vendors including Honeywell, Motorola, RCA, and others to identify available technical approaches and evaluate them with respect to technical merit, cost, availability of associated test equipment, hardware and software, and ease of implementation for production. Preliminary reliability and maintainability assessments have been made where possible. This report includes the results of the survey, along with a description and evaluation of the various approaches for implementation that the commercial vendors are considering.

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INTRODUCTION

A project to investigate an automatic test system was divided into two phases. Columbia Research Corporation (CRC), Arlington, VA, performed Phase I which was to review technical approaches and the feasibility of applying them to production. They also conducted a survey of the companies currently developing automated integrated circuit (IC) inspection systems. This report documents these findings. Phase II was intended to develop prototype inspection equipment based on the most promising and feasible approach identified in Phase I.

BACKGROUND

The family of scatterable mines (FASCAM) which includes remote antiarmor mine (RAAM), area denial artillery munition (ADAM), ground-emplaced mine scattering system (GEMSS), modular pack mine system (MOPMS), and GATOR mine system, currently uses large scale integrated circuits (LSIC) in their electronic fuzes. Defects in the LSIC can affect both the safe separation and self-sterilization features of FASCAM. Therefore, 100% visual inspection prior to encapsulation (pre-cap)[1] is required to prevent safety related defects, and would eliminate the time consuming use of microscopes and the subjectivity of human element present in the current inspection method. However, this costly, labor intensive inspection is not available from all semiconductor manufacturers to meet the program's needs.

Initial Status Meeting (ARRADCOM)

The following people attended an initial status meeting held at ARRADCOM, Dover, New Jersey on 2 October 1981: George Lutz and John Morgan, ARRADCOM, and Fran Erdle and Larry Reed, CRC. This meeting established the basic goals of the investigation. The difficulties to be expected in collecting information (e.g., the potentially proprietary nature of automated inspection systems development) were also discussed.

Electronics Design Week

A CRC engineer-investigator attended the Electronics Design Week held in Boston, Massachusetts to talk with representatives of Harris, Intel, Zilog, PMI, and other IC manufacturers. The CRC engineer-investigator collected literature and had informal discussions with attendees and manufacturer representatives concerning visual inspection.

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[1] MIL-STD-883, Test Method 2010.4, Test Methods and Procedures for Microelectronics.

Contact with Sources of Failure Rate Data

The following data centers were contacted for information on failure rates of LSICs and the possible existence of a causal relationship between the failures observed and the defects that should have been screened out by the pre-cap visual inspection: Rome Air Development Command (RADC), Nondestructive Test Center, National Bureau of Standards (NBS), and NASA Library.

Unfortunately, little information appears to be available concerning the failure rates of integrated circuits. The data that was uncovered was not of sufficient detail to allow for correlations to be drawn between observed failure modes and specific IC defects.

DISCUSSION

Current Status of the Pre-Cap Visual Inspection of the Timer Chip

The timer chip used on the ADAM and RAAM projects is considered a large scale integrated circuit (LSIC). It is specified a Class B microcircuit under MIL-M-38510 and is therefore inspected to Test Condition B of MIL-STD-883B, Test Method 2010.4. The timer chips are manufactured for Honeywell by RCA (Somerville, New Jersey) and Motorola (Austin, Texas). The chip produced by RCA is of a different configuration than that produced by Motorola (figs. 1 and 2).

Honeywell

Honeywell performs a destructive visual inspection of the ICs provided by RCA and Motorola on a sample basis as part of their incoming inspection process. The inspection is performed by operators with microscopes and the ICs are hand carried in trays to and from the inspection area. The visual inspection takes about six minutes per chip according to Honeywell. Removing the cap takes only a few seconds. The rejection rate is approximately 1%. The rejection rate for the overall screening process is about 15%. The defect information is recorded on travelers and stored for reference. The breakdown of the relative frequency of occurrence of each defect and the ability of the inspection to detect it is shown in table 1. No portion of the pre-cap visual inspection has been automated nor has there been any real attempt at automation.

Honeywell feels that the pre-cap visual inspection is a necessary quality assurance safeguard when microcircuit production is first starting. It takes time for the IC manufacturers to work the problems out of their production systems, and the visual inspection is a vital and effective screen at this point. As the quality of the product improves, however, the necessity and effectiveness of a 100% visual inspection, particularly one as stringent as Test Method 2010.4 tends to decrease.

RCA

At the RCA facility in Somerville, New Jersey, an inspector using a microscope performs the visual inspection. The ICs are transported to and from the inspection area in covered chip trays. There is a vacuum console for holding the wafer in place, and an indexer. Beyond that, no part of the system is automated, nor has there been any real attempt at automation.

The usual inspection line rate is approximately 77 ICs per hour. The inspection yield is approximately 85%. Defect information is fed back into the system. However, no long-term records of the relative frequency of each type of defect are maintained.

Motorola

Specific details on the Motorola inspection process were not received in time for inclusion in this report. However, the initial contacts show that the inspection involves an operator and a microscope, i.e., not an automated system. The predominant defects encountered appear to be passivation flaws, scratches, and foreign matter on the chip.

Current Status of the Pre-Cap Visual Inspection in Industry

The following firms were contacted and it was found that no automated visual inspection systems were currently in operation:

Alphatron, Incorporated
19080 Pruneridge Avenue
Cupertino, California 95014
(408) 446-1494

California Devices, Incorporated
282 Kinney Drive
San Jose, California 95112
(408) 295-3700

Fairchild Industries, Incorporated
Sherman Fairchild Technology Center
20301 Century Boulevard
Germantown, Maryland 20874
(301) 428-6000

Harris Corporation
Semiconductor Programs Division
P.O. Box 883
Melbourne, Florida 32901
(305) 729-5142

Omnibyte Corporation
245 W. Roosevelt Road, Building 1-5
West Chicago, Illinois 60185
(312) 231-6880

Precision Monolithics, Incorporated
1500 Space Park Drive
Santa Clara, California 95050
(408) 727-9222

Signetics Corporation
811 E. Arques Avenue
P.O. Box 409
Sunnyvale, California 94086

Sperry Corporation
Division Headquarters
Great Neck, New York 11020
(516) 574-2000

Mitel Corporation
P.O. Box 13089
Kanata, Ontario, Canada K2K 1X3
(613) 592-5280

TRW, Incorporated
Electronic Components Division
460 Totten Pond Road
Waltham, Massachusetts 02154
(617) 890-3232

The inspection was performed with an operator seated at a microscope. Harris Corporation had a conveyor system carrying the ICs to and from the inspection station, but the actual inspection was not automated. About two years ago experiments with a video system had been conducted and it was found to be very useful for training and for group viewing on marginal decisions. However, it did not improve the inspection process sufficiently to justify its cost and so was discontinued.

Engineering Studies and Evaluation

To allow a more comprehensive and objective evaluation of the alternative inspection procedures and of the positions taken by the various commercial vendors, CRC conducted engineering studies of the specific requirements of Test Method 2010.4. This included an in-depth investigation of the requirements and implications of visual inspection as defined by MIL-STD-883B along with a comparison with the requirements of MIL-M-38510 for military JAN microcircuits. The influence imposed by inspection controls can be estimated by comparing failure rate multipliers used for prediction from MIL-HDBK-217D.

Background

ICs provide a very large number of complete circuits on a single silicone wafer. Each circuit may contain hundreds of transistors, diodes, resistors, and capacitors, all interconnected by internal conductors, ending up at a small number of metal pads to which electrical connections from outside the device are made. The entire wafer is processed as a single component. When the metalization interconnection is completed each circuit is electrically tested, marked if bad, and finally the wafer is cut up into individual dies, each comprising a single circuit. From this point on, each circuit requires individual handling. Each good circuit die (rectangular chip of the original wafer) is bonded on a header of gold (Au) or aluminum (Al). Wires are bonded to the metal pads on the die and to the header terminals, precap tests and inspections are performed, and the encapsulation is finished by sealing.

A semiconductor integrated circuit can be fabricated using any of several existing technologies (bipolar, MOS, etc.). The steps in the fabrication process are different for each technology and different technologies are not usually combined in the same integrated circuit. Integrated circuits may also be classified according to functional classifications: linear circuits for both small signal and power use, digital circuits for logic use, and memory devices. An extremely rapid development is now occurring in IC technology which stems from several important causes:

1. Increased complexity of electronic circuitry

2. Reliability problems associated with complicated circuits of discrete parts

3. Need for reduction in operating power

4. Size and weight constraints

5. Costs

6. Ability of ICs to provide better solutions to system problems

ICs offer economic advantages to the user over and above their possible low initial cost. Since all the internal connections of the IC have already been performed in the fabrication process, relatively few interconnections are required to construct complex electronic systems. Assembly of a system from ICs rather than from equivalent discrete components involves the handling of fewer individual parts. Thus, the assembled system is much less expensive.

Systems using IC technologies also afford a low cost of ownership. The modular nature of ICs makes trouble-shooting and repair relatively simple. In addition, the reliability of ICs is considerably higher than that of circuits of discrete parts. The reasons for this include:

1. Fewer interconnections

2. Automated construction

3. Low physical and thermal mass

A more reliable system offers economic advantages in the long run over a less reliable system of larger or equal initial cost. In many cases, of course, reliability alone is the critical factor in determining whether a system is really useful.

High Quality and Reliability Microcircuits

For high quality and reliability levels, ICs are procured to meet requirements of MIL-M-38510. This specification establishes the design, quality, reliability assurance and vendor qualification and certification requirements for monolythic and hybrid microcircuits. There are three classes of screening established for military JAN microcircuits: MIL-M-38510, JAN Classes S, B, and C. Only microcircuits procured in full accordance with MIL-M-38510 may have the JAN designation.

The MIL-M-38510, Class S, B, and C microcircuits require screening tests in accordance with Method 5004 of MIL-STD-883B, Classes S, B, and C, respectively. A list of the screening procedures is shown in table 2. Manufacturers of JAN microcircuits must meet specific qualification requirements to acquire and

maintain listing on the qualified products list (QPL). This qualification requires a manufacturer certification (including a government approved Product Assurance Program Plan), production line certification, and qualification and quality conformance inspection testing.

Many microcircuits are procured to MIL-STD-883B, Class S, B, and C screening. Such devices may have been subjected to the test of MIL-STD-883B Method 5004.4 but have not had the in-process controls required by MIL-M-38510 and exhibit higher failure rates than MIL-M-38510 devices. Furthermore, there are various vendor equivalents, vendor classes, and lower grade commercial parts which exhibit still higher failure rates than both full MIL-M-38510 and MIL-STD-883 screened microcircuits. The extent to which failure rate is influenced by the imposed controls for each of the various quality grades can be estimated by comparing the failure rate multiplying factors used for predictions. The quality factors (π_Q) as published in the latest issue of MIL-HDBK-217 are shown in table 3.

Internal Visual Inspection

In order to meet one of the screening requirements of MIL-M-38510, microcircuits must be subjected to an internal visual inspection performed in accordance with MIL-STD-883B, Method 2010.4. The inspection is required prior to capping or encapsulation on a 100% basis to detect and eliminate devices with internal defects that could lead to device failure in normal application. Two test conditions are defined. Test condition A is intended for the ultra high reliability Class S microcircuits, and test condition B is intended for high reliability Class B and Class C microcircuits. In addition, certain substitutions and deviations are permitted on an optional basis in the case of complex microcircuits. These alternate methods and procedures are defined in paragraph 3.3 of MIL-STD-883B, Method 5004.4.

The internal visual inspection is but one of 17 screening tests required for each microcircuit supplied as a certified JAN product (table 2). While none of these screening procedures indicates how well or how long a device will perform in service, they do confirm whether the device meets its specifications after a series of exercises and tests. The array of tests includes burn-in, temperature cycling, thermal shock, acceleration, operating life tests, electrical tests before and after burn-in, particle impact noise detection, internal visual inspection after assembly, and a final electrical series of tests.

As an example (Method 5004.4, Test Condition B), the power burn-in test calls for operation at +125°C for a full week (160 hours) in order to eliminate what might appear to be electrically good devices, but which are actually marginal and subject to early failure under normal conditions. Such burn-in tests uncover metalization defects such as intermittent short or open circuits, pinholes in passivation layers beneath metalization, and corrosion or contamination defects. In active semiconductor regions, the power burn-in testing will disclose diffusion anomalies, oxide contamination, improper doping, and cracks in the die.

Temperature cycling tests similarly reveal changes in operating characteristics and physical dimensions as a function of temperature. The temperature is cycled from -65°C to +150°C. One cycle consists of 10 minutes at each extreme with a 5 minute transition time from one extreme to the other for a total of 30 minutes. The temperature cycling tests, thermal shock tests, and acceleration tests are useful in finding mechanical or physical weaknesses such as weak wire bonds, weak die bonds, cracked dies, and poor seals.

The internal visual inspection is performed just before the package is sealed. Under a microscope, die mounting, wire bonding, metalization conformity, oxide and diffusion quality, general mechanical integrity, and workmanship are confirmed. Visual inspection under a microscope is expected to find scratched metalization that may open in time, bonding problems that may result in short or open circuits, cracks or chips in the die, diffusion defects, pinholes, and passivation defects. Other problems that are uncovered by the microscopic visual inspection include contamination, corrosion, excessive etching, and the presence of foreign material imbedded in the chip layer or adrift in the package cavity.

This pre-cap, internal visual, screen for monolithic microcircuits as prescribed by Method 2010.4 is most comprehensive. The inspection details and procedures imposed under test condition B for JAN Class B certified microcircuits are shown in table 4. As shown in table 4, numerous categories of potential defects are explicitly targeted for exposure by an inspector, who must apply over a hundred separate items of rejection criteria, at a microscopic level of detail, to make each accept or reject decision. The inspection must be performed, depending on the character of the target defect, at either a high (75X to 100X) or a low (30X to 60X) level of magnification.

From a close examination of the many items of rejection criteria used in this screening procedure and knowing the topological details of current microcircuits having but a moderate level of complexity such as the timer chips, problems in the faithful performance of this manual inspection become apparent. The method used for visual screening consists of viewing a magnified portion of the microcircuit chip using a stereomicroscope and manually positioning the chip until all areas have been inspected. Because of the small field of view of microscopes at inspection stations, it is difficult and time consuming for the inspector. The technique is tedious and difficult to sustain for long periods of time because of eye fatigue and, unless great care is exercised, areas of the chip will be missed. Furthermore, these manual inspection techniques result in uneconomical production rates and increased procurement costs. In light of this, with microcircuit state-of-the-art and industry trends pushing the microcircuit chip circuit densities ever higher, into the thousands of gates per chip region, one must conclude that manual visual screens have become unfeasible.

Human Visual Inspection

MIL-STD-883B, Method 2010.4 requires inspection of microcircuits under optical magnifications as indicated. There are 15 different types of defects each with descriptions of the accept or reject criteria. These 15 items are as follows:

1. Thin film resistor contact area
2. Dielectric isolation defects
3. Balling of die attach material
4. Beam lead die faults
5. Beam lead bond area and location
6. Bonds at metalization exit
7. Bond dimensions
8. Bonding pad area
9. Passivation and diffusion faults
10. MOS gate alignment
11. MOS scratches and voids
12. Scribing and die defects (cracks)
13. Termination ends
14. Scratches
15. Voids

The inspector must scan the enlarged (magnified) chip image looking for flaws or defects. This scanning process is an orderly one which proceeds, for instance, from left to right and top to bottom, looking across some imaginary row and at each imaginary column within each row. The inspector then proceeds to the next row and the process is repeated. In each of these smaller areas of inspection, or row-column intersections, he or she must decide which types of defect could be present due to the particular configuration of the chip at this point. This action narrows the list of possible defects and simplifies the inspectors decision process. This action does require some time for accomplishment, however the total decision time would be considerably reduced, since the inspector must consider in each case not the entire list of 15 items, but a much reduced list, say 3 to 5 at the most.

At each stopping point of the visual scan the inspector must make a series of discriminations. These can be enumerated, for example, as follows:

1. Stop or proceed?
2. Which subgroup of defects could be present?
3. Is the defect present?

4. Is the defect less than minimal?

5. Is the defect more than minimal?

6. Accept or reject the chip?

7. Go on to next stopping point (or sub area)?

In the above listing, decisions 4 and 5 refer to the minimal presence of the defect. There are ten cases from the list of 15 that involve decisions in more than one dimension. In these cases the inspector has nine discriminations rather than the seven enumerated. For ease of calculations, we can assume that the possible defects are equally likely. Then we have an average of 8.333 discriminations per defect type. Let us assume that there are on the average four defect types per viewed cell. This would cause the inspector to repeat the defect detection decision process for each type of defect and result in 33.333 discriminations per cell.

Studies have been conducted in the area of how many discriminations the human can make in a given period of time.[2] The conclusions are that a human can make from 10 to 20 mental discriminations per second. These are cognitive processes related to the perception of retention of simple stimuli, such as those listed above. The variance is a function of fatigue. At the rate of 20 discriminations per second, the operator tires very rapidly. It has been concluded that an effective sustained rate of 18 discriminations per second is reasonable and quite achievable in practice, with breaks for relaxation.

Taking this figure, of 18 discriminations per second, with the specific data for this problem, that is 33.333 discriminations per stopping point. We see the operator could, on the average, inspect just over one half (18 divided by 33.333 = 0.54) stopping points per second or 1.852 seconds per cell. If we assume 10 rows and 10 columns and a chip size of 6 x 6 mm, then each of the areas to be inspected would be 0.6 x 0.6 mm. But, under 50X magnification, the inspector would be looking at an image 30 x 30 mm, or about an inch on a side, a reasonable area to be inspected in detail. At 100X magnification, the image being inspected would be about 2-1/2 inches on a side.

From the above we can see that a trained inspector could inspect one chip every 3 minutes, in accordance with MIL-STD-883B, Method 2010.4. This does not, however, account for the time required to position and repeatedly reposition the chip in the field of view of the microscope.

Another factor which must be considered when evaluating the human visual inspection is that not all of the defects are going to be detected. Two operators examining the same chip will detect different defects. Even the same operator looking at the same chip on two different occasions often will record different findings. The subsequent screening tests often uncover defects that should

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[2] J. M. Stroud, "The Fine Structure of Psychological Time" in the N.Y. Academy of Sciences Annals, 1967, 138(2), 623-631.

have been screened out by the pre-cap visual inspection. Thus, due to the complexities and sizes of today's LSICs, the human pre-cap visual inspection, in addition to being a time-consuming process, is limited in its ability to detect the defects it is designed to screen out.

Current Instruments and Systems for Increasing the Productivity and Effectiveness of the Inspection Process

So far, this report has looked at the inspection processes of the three timer chip manufacturers and other manufacturers of integrated circuits. It has analyzed MIL-STD-883B, Method 2010.4 and the ability of an inspector to perform this inspection. Now it is time to look at ways of improving the productivity and increasing the effectiveness of the inspection, while at the same time easing the burden on the inspectors.

Microscopes

Since the primary means of accomplishing this inspection currently involves an operator seated at a microscope, it seems logical to begin with an overview of what is available from the microscope manufacturers to make the inspector's task easier. The following microscope manufacturers were contacted to determine the state of the art in inspection microscopes:

Baush & Lomb
Scientific Optical Products Division
Rochester, NY 14692
(716) 338-6000

Olympus Corporation of America
Precision Instrument Division
4 Nevada Drive
New Hide Park, NY 11042
(212) 895-0843

Nikon Incorporated
Instrument Division
623 Steward Avenue
Garden City, NY 11530
(516) 222-0200

American Optical
Instrument Division
Box 123
Buffalo, NY 14240
(716) 895-4000

Vision Engineering, Incorporated
Kenosia Avenue
Danbury, CT 06810
(203) 744-7181

Applied Materials, Incorporated
Cobilt Division
3050 Bowers Avenue
Santa Clara, CA 95051

Adcotech Corporation
575 Maude Court
Sunnyvale, CA 94086
(408) 733-2820

Operations Technology, Incorporated
P.O. Box 276
Blairstown, NJ 07825
(201) 362-6200

Vickers Instruments, Incorporated
Riverview Business Park No. 27
300 Commercial Street
P.O. Box 99
Malden MA 02148
(617) 324-0350

Metron Optics, Incorporated
P.O. Box 690
Solana Beach, CA 92075
(714) 755-4477

Some of the microscope systems currently available appear in table 5. Each microscope has accessories available to tailor it to specific applications. Three of these special features would seem to be particularly useful in performing the pre-cap visual inspection.

Nomarski Differential Interference Contrast (DIC). Nomarski DIC is a specialized illumination attachment available on some of the microscope systems. This attachment highlights slight variations in surface quality. It does this by utilizing differences in grey color density or in interference colors. In this manner, the Nomarski DIC can indicate scratch depths and peak-to-peak heights.

Video Compatibility. Some of the microscopes already are compatible with closed circuit television (CCTV). Others have phototubes for camera attachments and could conceivably be adapted for CCTV use. A trinocular arrangement allows for simultaneous CCTV and binocular viewing with the majority of the light being fed to the video monitor. The use of video and CCTV in the inspection process is discussed under video and CCTV inspection equipment.

Automatic Transporters and Sorting Systems. Two inspection stations, the CI-750 by Applied Materials and the Series 3000-I by Adcotech, automatically transport the ICs to and from the station. In the CI-750, this is accomplished by means of belts, while in the Series 3000-I, the ICs are tube-fed. In both systems the operator indicates whether to accept, rework, or reject an IC. The sorting is then performed automatically and the information is stored in the system memory for later recall. The potential for damage to the ICs diminishes as the amount of handling decreases. The Applied Materials CI-750 is compatible with the Olympus microscope. The Adcotech Series 3000-I is video compatible.

Video and CCTV Inspection Equipment

The following manufacturers were contacted regarding ways of improving the basic inspection process by using video and closed circuit television inspection systems:

Automation Unlimited, Incorporated
10 Roessler Road
Woburn, MA 01801
(617) 933-7288

E. Leitz, Incorporated
Rockleigh, NJ 07647
(201) 767-1100

Boice Division
Mechanical Technology, Incorporated
968 Albany-Shaker Road
Latham, NY 12110
(518) 456-4131

Cambridge Instruments, Incorporated
40 Robert Pitt Drive
Monsey, NY 10952
(914) 356-3331

Colorado Video, Incorporated
Box 928
Boulder, CO 80306
(303) 444-3972

Daigger Scientific
10 Harbour Way
Richmond, CA 94801
(415) 233-6464

Delta Design, Incorporated
P.O. Box 421
San Diego, CA 92112
(714) 292-5000

Optoelectronics Systems Operation
General Electric Company
Building 3, Electronics Park
Syracuse, NY 13221
(315) 456-2832

Ham Industries, Incorporated
835 East Highland Road
Macedonia, OH 44056
(212) 467-4256

Hamamatsu Systems, Incorporated
332 Second Avenue
Waltham, MA 02254
(617) 890-3440

McBain Instruments, Incorporated
9175 Eton Avenue
Chatsworth, CA 91311
(213) 998-2702

Quantex Corporation
252 N. Wolfe Road
Sunnyvale, CA 94086
(408) 733-6730

Ryokosha Company, Ltd.
U.S. Distributor: Coberly & Assoc.
3350 Scott Boulevard
Building 47
Santa Clara, CA 95051
(408) 727-1530

Stocker & Yale, Incorporated
Route 128 & Brimbal Avenue
Beverly, MA 01915
(617) 927-3940

Technical Instrument Company
348 Sixth Street
San Francisco, CA 94103
(415) 431-8231

View Engineering, Incorporated
9731 Variel Avenue
Chatsworth, CA 91311
(213) 998-4230

Carl Zeiss, Incorporated
444 5th Avenue
New York, NY 10018
(212) 730-4400

General. Available video systems range in sophistication from simple CCTV equipment mounted on microscopes to image analyzers that can map dust particles on semiconductor chips. Video systems are employed at many stages of production to inspect raw materials, wafers, devices, circuit boards, and finished products. The technology has added accuracy and speed to both complex and simple inspection routines in many areas.

Several microscope manufacturers offer photomicrographic video equipment as options for their products. In the simplest arrangement, a TV camera is mounted on a trinocular microscope, and a video monitor is used to display the magnified image. The unit under test is thus magnified by the microscope lens and enlarged by the video system. Such systems are useful to reduce eyestrain or to allow more than one person to observe the unit under test. Multiple monitor hookups can also be arranged to carry the image to other locations. Instrumentation of this sort facilitates inspection in cases where low volumes do not demand automated techniques or where the object does not lend itself to inspection by any other method.

The TV systems enlargement or magnification is a function of the camera's picture tube diameter and the diagonal dimension of the monitor. This factor is multiplied by the microscope magnification to obtain the total magnification. For example, a one-inch camera tube, 13-inch monitor, and a 40X microscope objective yield a total screen magnification of 832X. A setup that provides such power can aid an inspector in making basic accept or reject decisions. For instance, shapes of incoming devices may be checked by comparing the video image of the sample with a mylar overlay affixed to the monitor. Deviations from the standard drawn on the mylar are readily apparent for non-complex items, and the inspector can make a go or no go judgment. If measurements are necessary, microscope manufacturers offer a variety of stage micrometers and reticles.

Just as video technology has enhanced microscope inspection techniques, optical comparators have been transformed into video comparators by the addition of two cameras and a monitor. While most optical comparators require special room illumination or an overhead canopy for a clear view of the projected image, video-based systems are freed from these constraints. Alternate images of the sample and the standard may be flashed on the monitor and errors show up as differences in color or motion between the views. Based on these differences, the inspector can assess the sample as good or bad. For closer inspection, both images can be displayed on a split or overlaid screen. Such instruments are in use inspecting high-density printed circuit boards used in computer and aerospace equipment.

In addition to the simplified, closed-loop video systems as described above, there are various methods of processing the video signal prior to display in order to enhance the image or evaluate its characteristics. Analog video signals from the camera tube can be converted to digital data that may be stored in computer memory or mass storage devices, or manipulated and conditioned in a number of ways to enhance clarity, identify perturbations and signal existence of deformities. Such image analysis instruments have generally been employed in fields outside of the electronic industry, such as material sciences for counting asbestos fibers and examining petrochemicals, and biomedical applications for ascertaining structure and character of cell tissue. There have been limited applications of image analyzers by semiconductor manufacturers for checking direct photolithography and particle contamination of wafers.

Equipment Availability. An extensive search, performed to determine the current availability of video inspection equipment, resulted in a list of 17 manufacturers. Each of the companies or their representatives were contacted and

the objectives of this project were discussed. The information received as a result of these discussions varies considerably in scope and detail; however, salient details follow:

1. Automation Unlimited, Inc. - The V80 Inspection System is a visual comparison system. The video camera scans the test unit along a preprogrammed path and displays the image on the screen alongside the stored image of a master. Thus, a direct, section-by-section comparison can be made by the operator. The system utilizes a Bausch and Lomb Microzoom microscope and has a combination digital printer and error code keyboard.

2. Boice Division of Mechanical Technology, Inc. - Boice's VISTA system employs a closed circuit TV camera to scan the part to be inspected and display an image on a video screen. The image is divided into about 65,000 elements for processing and storage. A part placed on the stage moves automatically into the field of view. The camera travels along the two axes to bring the item into focus. The instrument registers the image, which is digitized by the video processor. The data are then processed by software, and the measurements displayed on the display CRT. The equipment provides a rather large coordinate measuring surface and stage. Measuring ranges are available from 24 x 26 inches and up.

3. Cambridge Instruments - The QUANTIMET 900 image analyzing system represents one of the more sophisticated video analysis systems. Though the data received from Cambridge was of a sales brochure category, several salient facts were derived. The system application is more suitable to scientific or laboratory atmosphere. The microprocessor is a 16-bit RDP11/23 with a resolution of 896 x 704. Memory storage is 2 to 32 megabytes. The video scan rate is 10.5 frames per second. Video enhancement features are available, but no storage or retrieval processing times are given.

4. Colorado Video Inc. - A wide range of video system units are available for integration into custom-built applications. Video digitizers, video storage (memory) units (256 x 256 and 512 x 512 byte), video micrometers, video analyzers, and video display units.

5. Daigger Scientific - No information was received.

6. Delta Design Inc. - Provides an automatic video inspection system in general, low definition applications such as inspection of IC handling and marking operations, mechanical inspection, and lead and mask inspection.

7. General Electric Company - GE designs optoelectronic systems for control and inspection. These video inspection and processing systems have applications in surveillance, automated manufacturing, remote monitoring, process control, part sorting, and selection. Solid state camera resolution of 128 x 128 limits the field of view and thus throughput.

8. Ham Industries, Inc. - Using an overlay effect caused by alternately projecting the test unit image on the model or reference image, the CVC-3000 highlights such printed wiring assembly defects as missing, backwards, or incorrect components. Split screen is also available.

9. Hamamatsu Systems, Inc. - A broad array of building block units for a custom designed inspection system are offered, including video cameras having a wide range of characteristics, video frame memory, image analysis systems, area anlyzers, X-Y trackers, and semiconductor wafer inspection systems for particle contamination inspection.

10. E. Leitz, Inc. - Image analyzers and other microscopic video measurement systems are available. A sophisticated texture analysis system examines an entire frame and registers the number, size, distribution, form and orientation of structures essential to evaluate the quality of material.

11. McBain Instruments, Inc., - No information was received.

12. Quantex Corporation - Quantex offers a line of video image processors and filters. These devices perform various manipulation functions on digitally stored video data to enhance otherwise unsuitable video images.

13. Ryokosha Company - Ryokosha manufacture a line of high-powered, semi-automatic video comparator systems. Basically the system is a video-enhanced microscopic micrometer.

14. Stocker & Yale, Inc., - No information was received.

15. Technical Instrument Company - No information was received.

16. View Engineering - VISION 85, by View Engineering, is a general pattern recognition system that retrofits wire bonders, saws and wafer probers. The system does not process an entire video frame, but a manageable number of points are entered into the program. Precision location is afforded in microcircuit fabrication operations. The reference area used is contained in a 64 x 64 pixel matrix.

17. Carl Zeiss, Inc. - The IBAS interactive image analysis system is a fully automatic image analysis and image processing system for research and routine microscopic anlaysis work. It has a high resolution, 512 x 512 pixels, each with a 256 level gray scale. Memory is available in 1 megabyte steps to a total of 16 megabytes.

Automated Inspection Systems

The following manufacturers of automated test equipment (ATE) were contacted to see if they currently had or were developing an automated system to perform the pre-cap visual inspection:

Advanced Microtechnology, Inc.
480 Mercury Drive
Sunnyvale, CA 94086
(408) 736-3860

Contrex, Inc.
Burlington, MA
(617) 273-3434

Aerotronic Associates, Inc.
Contoocook, NH 03229
(603) 746-4631

ATE Associates, Inc.
5707 Corsa Avenue
Westlake Village, CA 91362
(213) 991-4001

A.T.E. Systems, Inc.
10 Dale Street
Waltham, MA 02154
(617) 800-9614

Bendix Corporation
Test Systems Division
Teterboro, NJ 07608
(201) 288-2000

JRM Electronics
P.O. Box 135
Vincentown, NJ 08088
(609) 859-2106

KLA Instruments Corporation
2051 Mission College Boulevard
Santa Clara, CA 95054
(408) 988-6100

Test Engineering Solutions, Inc.
19234 Vanowen Street
Reseda, CA 91335
(213) 708-0390

Testmaster, Inc.
3191-D Airport Loop Drive
Costa Mesa, CA 92626
(714) 754-0225

To date, however, no one has such a system available on the market. Details about these systems are difficult to obtain because they are still in the development stage and much of the information is proprietary.

KLA Instrument Corporation. KLA Instrument Corporation of Santa Clara, California currently is working on an IC inspection system. This system apparently utilizes image comparison techniques between the test chip and a master reference chip. The difficulty with developing such an inspection system is that the requirements of Method 2010.4 push the state-of-the-art in software capabilities. It is one thing to design a system that can automatically perform the inspection. It is another to design one that is cost-effective. At present, KLA is using a general purpose computer which is not fast enough to show large decreases in inspection times, although it is still faster than human inspectors. KLA hopes to improve this by custom-making the computer to better serve the system. The development process has not yet reached the point where there is any printed information ready for release.

Hitachi. In Japan, Hitachi is reportedly working on an automated visual inspection system for ICs. No details are available about the system other than Hitachi estimates that it will be about two years before its system will be ready to market.

Contrex. Contrex, Inc., of Burlington, Massachusetts, has been developing a fully automated chip inspection system (CIS) which utilizes a technique called image understanding. Image understanding can be thought of as the capability of a computer to extract, process, and interpret, in real time, visual information provided by an image acquisition device such as a CCTV camera. The CIS is made up of the following design elements:

- System controller, with custom software for chip inspection, error reporting and tabulation.

- Image analyzer, which converts the viewed image into a digitized form, extracting the features needed in the decision making process.

- Operator console, which allows manual entry of data and manipulation of the various electromechanical components of the system. The console also includes a videomonitor for reviewing the progress of the tests and for operator prompting.

- Optical microscope, with computer controlled Z-axis movement for automatic focusing.

- An X, Y, Theta positioning stage, allowing reproducible positioning of the chip under test to 0.0001 inch. This positioner is also controlled by the system controller via the imaging feedback loop.

- Computer controllable illumination system, which allows the system controller to maintain a constant level of illumination over the span of the test. It also enables the system to reproduce the level of illumination from one test run to a new test run some period of time later, without requiring manual intervention.

Learning Process. With the aid of the operator, the special visual properties of the chip are analyzed by the inspection system. Such features as pad locations, chip active area, chip outer area, chip geometry, and areas where no testing is desired are entered. Proper light levels and focus are stored to ensure identical conditions. Reference data such as chip type, serial number, and manufacturer are also entered. The learning process for a typical chip is between 3 to 5 minutes depending on chip complexity and data entry requirements. There is no additional learning-curve process. All relevant data concerning each chip type is entered only once and maintained for future reference.

Inspection Process. The CIS performs a three-stage inspection. The stages are as follows:

1. Course Screening. This quick-scan mode provides rapid verification of batch quantity and gross geometric features.

2. Major Defect Screening. This medium-level mode of inspection is designed to eliminate all chips with major defects, such as chipouts, scratches and cracks, dirt and contamination, pad corrosion and discoloration, and pad defects due to multiple probe marks. The level of magnification at this stage allows discrimination of defects of 0.5 mil or greater.

3. High Resolution Screening. This final stage is designed to uncover such defects as metalization voids and bridging, misalignment of contact windows, and passivation faults. The magnification at this stage must be capable

of providing safe discrimination of a 50% narrowing of a metal trace. All of the defects uncovered are logged and stored for easy retrieval.

The Contrex CIS is still undergoing development. However, one such system has been developed for ILC Data Device Corporation in Bohemia, New York.

Other Current Techniques with Possible Application to Pre-Cap Visual Inspection

Although there is no work currently being done to develop them for this purpose, the following techniques have been evaluated regarding their potential application to pre-cap visual inspection. They are techniques to be watched in the future.

Laser Optics

Several companies are working on automated systems for the visual inspection of printed circuit boards. In these efforts, laser technology has proven to be a useful tool.

Chrysler. The Chrysler Electronics Division in Huntsville, Alabama has developed the LIS-510 inspection system which utilizes a low power helium-neon laser, an X-Y moving iron galvanometer scanner, and several folding mirrors. By scanning over a pre-programmed path the system produces unique shadow signatures which are picked up by silicon photodiodes. These signals are evaluated by a minicomputer which also controls the scan pattern.

The LIS-510 system is capable of automatically detecting missing components, incorrect lead clinch direction, and improper lead length (long and short). With the use of a reflective glint screen, solder bridges can also be detected. This system is better than 99% effective in detecting board faults on the Chrysler production line. It can inspect a 400-lead board for component presence and proper lead dress in less than 5 seconds. It can scan a bare board for improperly sized or placed component holes at a minimum rate of 50 holes per second.

Altman Associates. The Altman Associates, Stamford, Connecticut, board verifier system also analyzes reflected laser beams from the test board to check hole sizes and positions. However, this system does not utilize a master pattern stored in its memory. In its place, a second beam from the laser scans artwork that describes the nominal tolerances of the board. The minicomputer then decides if the features of the test board come within the allowed tolerances. This system allows the inspection of different board types without reprogramming. The predicted inspection rate is up to 50 square feet of bare board per minute with measurement accuracies to within 1 mil.

Cooper Industries. The Inspectron system by the Advanced Control Products division of Cooper Industries in Irvine, California is predicted to take about one minute to inspect a bare board for line widths and spacing, line breaks, excess copper, and voids. The system will also detect incomplete pads, poor pad-lead connections, and shorts in ground planes. The Inspectron utilizes reflected laser beams in analyzing these board features, but its only reference is a set of design rules programmed into its minicomputer. When a violation is detected, the system will either print out the coordinates of the defect or stop scanning so an operator can examine the defect. The use of general design principles instead of master pattern or artwork references eliminates the need for precise orientation of the test board. This system is still in the development stage.

Vanzetti Infrared and Computer Systems. Also in the development stage is a unique solder joint inspection system from Vanzetti Infrared and Computer Systems in Canton, Massachusetts. This system utilizes infrared rather than visible light detectors. The laser delivers low-power pulses to each joint, heating it a few degrees above the temperature of the room. The minicomputer then compares the joint's thermal response and makes a pass or fail decision. For example, a joint with insufficient solder or a subsurface void will warm up faster and reach a higher peak temperature than will a good joint. Thus, this system can pinpoint faults that a human inspector would be unable to detect.

Summary. None of these systems, in their present forms, is capable of performing the pre-cap visual inspection described in Method 2010.4. The pre-cap inspection is too complex and the ICs are too small. However, lasers are capable of very high resolution and pinpoint accuracy. It may simply be a matter of thinking of the inspection problem in terms of lasers.

Acoustic Microscopy

The acoustic microscope allows an inspector to see minute structural details of an object by displaying the object's response to ultrasonic waves. Unlike optical microscopes, they are capable of probing beneath the visible surface. The acoustic microscope displays the changes in the efficiency with which sound is generated in or propagated through the item being inspected. The physical properties of the object, such as density, viscoelastic moduli and thermoelastic coefficients, determine the sonic speed, dispersion and refraction of the sound waves. Thus, when reflected or transmitted sound waves are enlarged and displayed, an accurate picture of the target is produced. This display will include those portions of the item which are optically opaque, allowing the inspector to see within or beyond these areas. The system consists of two basic parts. One exposes the object to the ultrasonic radiation and the other senses and displays the resulting acoustic fields. The acoustic microscopes investigated differ in the manner in which they expose the inspected object to the ultrasonic radiation. The image-conversion and image-display systems are very similar to each other and are widely used in many other imaging systems.

An acoustic microscope, known commercially as SONOSCAN, has been available since 1975. In this system a sound wave is passed through the inspected item, which is mounted in a liquid cell. On the far side of the liquid cell is an optical mirror. The sound wave passes through the mirror causing it to vibrate. This vibration is detected and measured by a focused laser beam which is phase modulated by the vibration. A scanning mechanism moves the beam over the surface of the mirror in a regular manner, creating a raster pattern which is repeated at television frame rates. The reflected phase modulated light is changed to intensity modulated light by an optical modulation converter and then projected onto a photoelectric detector. The output of the photoelectric detector is presented to the image-display system. The resolution of this system is a function of the size of the light spot and the mirror physics. A practical system can employ a light spot with a diameter of 1.5 acoustic wavelengths. This system is available from Sonoscan, Inc. of Bensenville, Illinois.

Leitz, Federal Republic of Germany, and Olympus, Japan, are in the process of developing acoustic lens microscopes employing techniques devised at Stanford University. These systems employ two transducer assemblies, separated by a cell filled with a liquid in which the inspected object is mounted. The transducer assemblies each consist of a sapphire rod with a piezoelectric transducer at one end. The other end is ground into a concave spherical surface to form the lens. The inspected object must be mounted at the common focal point of these two facing concave surfaces. An ultrasonic beam is mechanically scanned in a raster pattern from the transmitting transducer through its sapphire rod and lens, through the object being inspected, and into the receiving transducer via its sapphire rod and lens. This output is fed to the image-display system. The resolution of this system can approach one half of the ultrasonic wave in the liquid, but the cell must be kept thin. For practical operating frequencies of 1.5 GHz, resolutions of one half micrometer can be obtained.

IBM and Livermore Laboratories have recently reported a third type of acoustic microscope. This system utilizes either a moving intensity modulated laser or electron beam to generate ultrasonic beams from a large area acoustic source after passing through the object to be inspected. This process is approximately the reverse of that utilized by the SONOSCAN. These systems produce sound when in scanning an object, the intensity modulated electron or laser beam is absorbed by the object. The particular absorption depends upon the thermoelastic response and the heating at that point. The display of these microscopes quantitatively describes the thermoelastic properties, as modified by the absorption coefficient for light or electrons and by the object's beam spreading characteristics. The raster pattern output of the piezoelectric transducer is fed to the image-display system. Resolution of this system is dependent upon the spot size of the electron or laser beam, beam spread, and thermal diffusion of the beam caused by the heating of the object.

In each acoustic microscope described above, an image-display system is required. This is commonly a television-type picture on a CRT, but the raster pattern can be directly printed by a camera on film. Electronic image processing can be incorporated to enhance or enlarge the image or to extract specific information. Electronic pattern recognition or comparison could be employed to automate the accept or reject decision.

The SONOSCAN and the acoustic lens techniques have the decided drawbacks of the liquid immersion of the inspected object and the very small size (thickness) of the cavity available for insertion of the item. However, their resolutions are quite good. The SONOSCAN's resolution is about equal to a good optical microscope, while the acoustic lens is about three to four times lower. The third technique, while not as fully developed as the other two, shows more utility for microcircuitry inspection. However, the source excitation frequency must be high enough to generate an acoustic wave at a wavelength comparible to the detail of interest. Wavelengths of from 5 to 0.03 micrometers in metals and thermal insulators are quite reasonably achievable.

Electro-Optical Pattern Recognition

Perkin-Elmer Corporation has developed an automatic electro-optical pattern recognition system for the Bureau of Engraving and Printing. The developmental model of this equipment is currently being used to inspect sheets of U.S. currency. Each new bill is compared electronically to a master reference bill whose image is stored in a computer. The images are compared on a pixel by pixel basis. Flaw descrimination is accomplished by generating exceedance data for each pixel (the positive or negative difference between the features of the examined pixel and those of the stored master pixel). Computer algorithms determine the reject criteria for the note as a whole. The scan head that examines the notes is a charged-coupled device (CCD) detector. It has 1024 photosites, with two adjacent sites representing a single pixel. Thus each pixel is 0.3 mm square. For each pixel a four-bit digitized word is generated representative of that 0.3 x 0.3 mm pixel. There are eight scan heads in line allowing simultaneous inspection of eight bills. This facility inspects the front and back of 6000 sheets of bills, 32 to a sheet, in one hour. A significant part of the equipment, hardware and software, is involved in transporting, aligning, registering, flipping, sorting, and stacking the sheets of bills. Such a device could be adapted to the examination of magnified images of integrated circuit chips and making a pixel by pixel comparison with a perfect master image.

CONCLUSIONS

Based upon CRC's investigation of the pre-cap visual inspection and the current efforts to automate the process, the following conclusions have been reached:

Evaluation of the Internal Visual Inspection

The internal visual inspection of integrated circuits is a very involved procedure. As integrated circuits continue (as they will) to become smaller and more complex, the probability of a defect being detected by a visual inspection will decrease. The exception would be gross physical defects which would probably be detected in later screening tests anyway.

The fact that this is a human visual inspection gives rise to further problems. First of all, there is a limit to the speed with which an operator can perform the inspection. Second, in any human inspection a certain number of rejects are going to slip through. This number increases as the inspection rate goes up. Finally, there is the problem of subjectivity in the inspection. What one operator would reject, another might pass. Thus, the speed and effectiveness of the inspection is degraded by the fact that it is performed by humans, and this degradation can be expected to become more pronounced as the complexity of the integrated circuit increases.

Availability of Automated Inspection Systems

None of the IC manufacturers contacted by CRC currently have available an automated system to perform the pre-cap visual inspection. Few of the instrument manufacturers are even working on it. The primary reason given for this is that the inspection itself is so complex. Three manufacturers (KLA, Hitachi, and Contrex) appear to be attempting to automate the inspection process. These systems are discussed in the section entitled Automated Inspection Systems. Detailed information is not available at this point because the systems are still in the development stage, and much of the information is proprietary. Thus, a best-buy prediction, even among these systems, cannot be made at this time. Also, there may still be other systems under development that have not come to the attention of CRC in the course of the survey.

Now that it has been determined that there is work being done on automating the visual inspection and that there are other techniques that could be applied to the task, the next logical step would be the determination of which method would best serve the purpose of performing the inspection in the most efficient manner. The most direct method of obtaining the information required to make such a decision is to issue a Request for Proposal (RFP). It would then be in the interest of each vendor to provide a detailed description of his process, including cost information and a time-frame for installation of the system. A RFP, in addition to obtaining more detailed descriptions of the systems highlighted in this report, would attract any companies currently developing inspection systems that our investigation may have overlooked.

Further Studies Required

The purpose of the Scope of Work developed by ARRADCOM for this project (appendix) was, in part, to resolve concerns about the need for the visual inspection itself. The frequency of occurrence, consequence, and difficulty of inspection of each defect type became relevant factors when the inspection effectiveness and necessity are in doubt. Therefore, the real thrust of future studies should be directed toward answering the following two questions:

1. Is the pre-cap visual inspection really necessary?

2. Is the selected automated inspection system comparable or superior to the human visual inspection?

Verification of the Need for the Pre-Cap Visual Inspection

Probably the most straightforward method of verification involves simply marking the ICs that fail the pre-cap visual inspection and then allowing them to continue through the remainder of the screening process. If such an IC fails a subsequent screening test, such as a burn-in, it is removed and the cause of failure recorded for comparison with the original defect. If any of the tagged ICs make it through the battery of screening tests, this may be construed as justification for keeping the inspection. If however, all of the visually defective chips are picked up on subsequent testing, the inspection would appear to be unnecessary and serious consideration regarding its discontinuation would be warranted.

Evaluation of the Automated Inspection System. That an automated inspection system can perform the task more quickly than its human counterparts is only half of the solution. The automated system must also demonstrate the ability to detect IC defects at least as well as, and preferably better than, a human inspector. A test method which could be used to evaluate the automated inspection system requires the sequential inspection of a large sample of ICs by both the human and automated methods.

Data taken during the test includes the pass-fail status of each IC for each inspection. This information can be displayed in an array as follows:

	All Chips		
Inspection	Pass %	Fail %	
Visual			$\Sigma = 100\%$
Automated			$\Sigma = 100\%$
Both			$\Sigma < 100\%$

The category designated as "both" includes only those chips that pass or fail both inspections. A matrix comparing the chips failed by each inspection is also established as follows:

	Automated		
Visual	Pass %	Fail %	
Pass %			$\Sigma = 100\%$
Fail %			$\Sigma = 100\%$
	$\Sigma = 100\%$	$\Sigma = 100\%$	

The data obtained in the test is then subjected to a statistical analysis from which the better system can be determined. This analysis should provide answers to the following questions:

1. Is there a significant difference between the screening performances of the two methods?

2. On a statistical basis, are there any defect types overlooked by one system which are detected by the other?

3. To what extent is the effectiveness of each inspection process influenced by the rate of throughput?

CRC's report and follow-up contacts by ARRADCOM indicate that there are no commercial contractors who have developed and installed equipment for routine inspection on a production basis. The necessary equipment is in a preliminary development stage where concepts and implementation are in the process of design and evaluation. Therefore, because of the current technological state of the art, the project was terminated at the end of Phase I.

RECOMMENDATIONS

It is recommended that the following actions be taken to resolve questions unanswered by the present survey and to provide important additional information required by ARRADCOM to make an informed technical decision as to the feasibility and cost-effectiveness of automating the pre-cap visual inspection of integrated circuits:

1. A thorough evaluation of the necessity and effectiveness of the pre-cap visual inspection should be undertaken. As part of this evaluation, the IC manufacturers should be tasked to tag the chips failing the visual inspection and then allow them to continue through the screening process to see if they are detected in subsequent tests.

2. In order to obtain the detailed information on cost and predicted availability required to make a best-buy determination regarding an automated test system, a Request for Proposal should be issued for the establishment of such a system.

3. In order to verify the superiority of the automated system to the human visual inspection, a test program should be established, in cooperation with the IC vendors, in which a large sample of chips is inspected sequentially by both systems. A statistical analysis should be performed on the resulting data to compare the relative screening effectiveness of the automated and human systems.

The progress of private industry (KLA Instrument Corporation and Contrex, Inc.) engaged in the research and development stages of this technology should be monitored. If techniques become available, a future MTT project to adapt them to specific components of interest to the Army should be pursued.

Table 1. Relative frequency of defect occurrence per (MIL-STD-883B, Method 2010.4) and probability of detection

Defect Category	Occurrence	Probability of Detection
SECTION 1. Metallization Defects		
Metallization Scratches	4	2
Metallization Voids	2	4
Metallization Corrosion	5	4
Metallization Adherence	3	5
Metallization Bridging	3	5
Metallization Alignment	4	4
SECTION 2. Oxide and Diffusion Defects		
Oxide and Diffusion Bridging	5	3
Diffusion Less Than 25% of Nominal Width	5	3
Oxide Absence Under Metallization	5	5
SECTION 3. Scribing and Die Defects		
Less than 0.1 Mil Oxide on Periphery of Chip	4	1
Chip of Crack in Ckt	4	1
Crack Greater Than 5 Mils in Length	4	3
Cracks Towards Metal	4	5
SECTION 4. Bond Defects		
Ball Bonds Misdimensioned	3	2
Ball Bonds Missing Pad Area	4	2
Ball Bonds Asymetrical	5	5
Wedge Bonds Misdimensioned	4	2
Wedge Bonds Missing Pad Area	4	2
Wedge Bond Wires Crossing	5	1
Bond - Metal Separation	4	4
Bonds in Fillet Area	5	4
Wire Tails	3	4
SECTION 5. Wire Defects		
Excessive Wire	5	5
Nicked, Cut Wires	3	5
Missing or Extra Wires	5	2
Wire Torn From Bond	5	4
SECTION 6. Foreign Material and Mount Defects		
Unattached Foreign Materials	2	2
Attached Conductive Foreign Materials - Shorts	4	2
Die Mounting Material on Top of Ckt.	4	1
Die to Header Melt not Visible	4	5
Balling or Flaking of Die Mount Material	5	4

Key

Defect Occurrence

1. Common
5. Rare

Probability of Detection

1. Probable
5. High Risk

Table 2. Integrated circuit screening requirements as designated in MIL-STD-883B, Method 5004.4

Screen	Class S		Class B		Class C	
	Method	Reqmt	Method	Rsqmt	Method	Reqmt
3.1.1 Internal visual 1/	2010, test condition A	100%	2010, test condition B	100%	2010, test condition B	100%
3.1.2 Stabilization bake (see 3.4.1, 3.4.2) no end point measurements required	1008 24 hrs, min, test condition C min	100%	1008 24 hrs, min, test condition C min	100%	1008 24 hrs, min, test condition C min	100%
3.1.3 Temperature cycling 2/	1010, test condition C	100%	1010, test condition C	100%	1010, test condition C	100%
3.1.4 Constant acceleration (see 3.2 and 3.4.2)	2001, test condition E (min) Y_1 orientation only	100%	2001, test condition E (min) Y_1 orientation only	100%	2001, test condition E (min) Y_1 orientation only	100%
3.1.5 Visual inspection 3/		100%		100%		100%
3.1.6 Seal 4/ (a) Fine (b) Gross	1014	100% 5/	1014	100%	1014	100%
3.1.7 Particle impact noise detection (PIND)	2020, test condition A or B	100% 6/		----		----
3.1.8 Serialization		7/		----		----
3.1.9 Interim (pre-burn-in) electrical parameters (see 3.5.1)	Per applicable device specification	100% 8/	Per applicable device specification	9/		----

Table 2. (cont)

	Class S		Class B		Class C	
	Method	Reqmt	Method	Reqmt	Method	Reqmt
3.1.10 Burn-in test (see 3.4.2)	1015 10/	100%	1015	100%		----
3.1.11 Interim (post-burn-in) electrical parameters (see 3.5.1)	Per applicable device specification	100%		----		----
3.1.12 Reverse bias burn-in 11/ (see 3.4.2)	1015; test condition A or C, 72 hrs @ 150°C min 10/	100%		----		----
3.1.13 Interim (post-burn-in) electrical parameters (see 3.5.1)	Per applicable device specification	100% 8/	Per applicable device specification	100%		----
3.1.14 Seal (a) Fine (b) Gross	1014	100%		----		----
3.1.15 Final electrical test (see 3.5.2) (a) static tests (1) 25°C (subgroup 1, table I, 5005) (2) Maximum and minimum rated operating temp.	Per applicable device specification	100% 100%	Per applicable device specification	100% 100%	Per applicable device specification	100% 100%

Table 2. (cont)

	Class S		Class B		Class C	
	Method	Reqmt	Method	Reqmt	Method	Reqmt
(subgroups 2, 3, table I, 5005) (b) Dynamic tests and switching tests 25°C (subgroups 4 and 9, table I, 5005) (c) Functional test 25°C (subgroup 7, table I, 5005)		100% 100%		100% 100%		100% 100%
3.1.16 Radiographic 12/	2012 two views	100%		----		----
3.1.17 Qualification or quality conformance inspection test sample selection		13/		13/		13/
3.1.18 External visual	2009	100%	2009	100%	2009	100%

1/ Unless otherwise specified, at the manufacturer's option, test samples for group B, bond strength (method 5005) may be selected randomly immediately following internal visual (method 5004) prior to sealing.

2/ For class B and C devices, this test may be replaced with thermal shock method 1011, test conditior A, minimum.

3/ At the manufacturer's option, visual inspection for catastrophic failures may be conducted after each of the thermal/mechanical screens, after the sequence or after seal test. Catastrophic failures are defined as missing leads, broken packages or lids off.

4/ For classes B and C devices, the seal test may be performed in any sequence between 3.1.6 and 3.1.16, but it shall be performed after all shearing and forming operations on the terminals.

5/ Optinal when 3.1.14 is performed.

6/ See MIL-M-38510 paragraph 4.6.3. The PIND test may be perfromed in any sequence after 3.1.4 and prior to 3.1.13.

7/ Class S devices shall be serialized prior to interim electrical parameter measurements.

8/ Electrical parameters shall be read and recorded.

9/ When specified in the applicable device specification, 100 percent of the devices shall be tested for those parameters requiring delts calculations.

10/ For class S devices, test condition F of method 1015 and 3.4.2 herein shall not apply.

11/ The reverse bias burn-in (see 3.1.12) is a requirement only when specified in the applicable device specification and is recommended only for certain MOS, linear or other microcircuits where surface snesitivity may be of concern. When reverse bias burn-in is not required, interim electrical parameter measurements of 3.1.11 are omitted. The order of performing the burn-in (see 3.1.10) and tha reversa bias burn-in may ba inverted.

12/ The radiographic (see 3.1.16) screen may be performed in any sequence after 3.1.8.

13/ Samples shall be selected for testing in accordance with the specific device class and lot requirements of method 5005.

Table 3. π_Q, quality factors (per MIL-HDBK-217D)

Quality Level	Description	π_Q
S	Procured in full accordance with MIL-M-38510, Class S requirements.	0.5
B	Procured in full accordance with MIL-M-38510, Class B requirements.	1.0
B-0	Procured in full accordance with MIL-M-38510, Class B requirements except that device is not listed on Qualified Products List (QPL). The device shall be tested to all the electrical requirements (parameters, conditions and limits) of the applicable MIL-M-38510 slash sheet. No waivers are allowed except current and valid generic data** may be substituted for Groups C and D.	2.0
B-1	Procured to all the screening requirements of MIL-STD-883, Method 5004, Class B and in accordance with electrical requirements of MIL-M-38510, DESC drawings, or vendor/contractor electrical parameters. The device shall be tested to all the quality conformance requirements of MIL-STD-883, Method 5005, Class B. No waivers are allowed except current and valid generic data** may be substituted for Groups C and D. This category applies to DESC drawings and contractor prepared specification control drawings (SCD's) containing the above B-1 screening and quality conformance requirements.	3.0
B-2	Procured to vendor's equivalent of the screening requirements of MIL-STD-883, Method 5004, Class B, and in accordance with the vendor's electrical parameters and vendor's equivalent quality conformance requirements of MIL-STD-883, Method 5005, Class B. Applies to contractor conformance requirements.	6.5
C	Procured in full accordance with MIL-M-38510, Class C requirements.	8.0
C-1	Procured to screening requirements of MIL-STD-883, Method 5004, Class C and the qualification requirements of Method 5005, Class C. Generic data may be substituted for Groups C and D.	13.0
D	Hermetically sealed part with no screening beyond the manufacturer's regular quality assurance practices; parts encapsulated with organic material.*	17.5
D-1	Commercial (or non-mil standard) part, encapsulated or sealed with organic materials (e.g., epoxy, silicone or phenolic).	35.0

* All encapsulated devices must be subjected to 160 hr. burn-in at 125°C., 10 temperature cycles (-55°C to 125°C) with end point electricals, and high temperature continuity test at 100°C.

** Group C generic data must be on data codes no more than one year old and on a die in the same microcircuit group (see Appendix E of MIL-M-38510) with the same material, design and process, and from the same plant as the die represented. Group D generic data must be on data codes no more than one year old and on the same package type (see 3.1.3.12 of MIL-M-38510) and from the same plant as the package represented.

Table 4. MIL-STD-883B internal visual (monolithic) screens, Method 2010.4 Class B requirements

Explanation of Column Headings and Contents Listed at End of Table, Page

a. 2010.4 Para. No.	b. Defect Category	c. Magfn.	d. Altern.	e. Rejection Criteria	f. Potential Failure Mode	g. Difficulty	h. Criticality
3.2.1	Metallization Defects:						
3.2.1.1	Metallization Scratches	High	Low	a. Scratch in the metallization excluding bonding pads, that exposes underlying passivation anywhere along its length and leaves less than 50% of the original metal width undisturbed.	Open	3	3
				b. Scratch that completely crosses a metallization and damages the surface of the surrounding passivation or glassivation on either side. (For MOS devices, the path shall be the (L) dimension.	Open	3	4
				c. Scratch in multilayered metallization that exposes the underlying metal anywhere along its length and leaves less than 25% of the top-layer original metal width undisturbed.	Open	3	3
				d. Scratch in the metallization over a passivation step that leaves less than 75% of the original metal width at the step undisturbed.	Open	3	2
				e. Any scratch in the metallization, over the gate oxide bridge, that exposes underlying passivation and leaves less than 50% of the length or width of the metallization between source and drain diffusion undisturbed (applicable to MOS structures).	Loss Of Function	4	3
				f. Scratch in the metallization that exposes the dielectric material of a thin film capacitor or crossover.	Open	4	2
				g. Scratch in the bonding pad or fillet area that exposes underlying passivation and reduces the metallization path width connecting the bond to the interconnecting metallization to less than 50% of the narrowest entering interconnect metallization stripe width. If two or more stripes enter a bonding pad, each shall be considered separately.	Open	3	3
				h. Scratch(es) (probe mark(s), etc.,) in the bonding pad area that exposes underlying passivation over more than 25% of the original unglassivated metallization area.	Open	2	2
3.2.1.2	Metallization Voids	High	Low	a. Void(s) in the metallization that leaves less than 50% of the original metal width undisturbed.	Open	3	3
				b. Void(s) in the metallization over a passivation step that leaves less than 75% of the original metal width at the step undisturbed.	Open	3	2
				c. Void(s) in the metallization over the gate oxide bridge that leaves less than 75% of the metallization length (L) between source and drain diffusions undisturbed.	Loss Of Function	4	2

Table 4. (cont)

a. 2010.4 Para. No.	b. Defect Category	c. Magfn.	d. Altern.	e. Rejection Criteria	f. Potential Failure Mode	g. Difficulty	h. Criticality
3.2.1	Metallization Defects:						
3.2.1.2	Metallization Voida (continued)			c. (applicable to MOS structures).			
				d. Void(s) that leave less than 60% of the metallization area over the gate oxide bridge undiaturbed (applicable to MOS structures).	Loss Of Function	4	3
				e. Void(s) that leaves less than 75% of the metallization width coincident with the source or drain diffusion junction line, undisturbed (applicable to MOS structures).	Loss Of Function	4	3
				f. Void(s) in the bonding pad area that leaves less than 75% of its original unglassivated metallization area undiaturbed.	Open	2	2
				g. Void(s) in the bonding pad or fillet area that reduces the metallization path width connecting the bond to the interconnecting metallization to lesa than 50% of the narrowest entering interconnect metallization stripe width.	Open	3	2
				h. Void(s) in the metallization of a thin film capacitor that reduces the metallization area by more than 25%.	Capacity Reduction	4	2
3.2.1.3	Metallization Corrosion	High	Delete	a. Any metallization corrosion.	Leakage	2	N
3.2.1.4	Metallization Adherence	High	Delete	a. Any metallization lifting, peeling or blistering.	Open Or Short	2	4
3.2.1.5	Metallization Probing	High	Delete	Criteria contained in 3.2.1.1 shall apply...			
3.2.1.6	Metallization Bridging	High	Delete	a. Any metallization bridging where the separation between any two metallization paths is reduced to less than 0.1 mil.	Short	3	4
3.2.1.7	Metallization Alignment	High	Delete	a. Contact window that has less than 50% of its area covered by metallization.	Open	2	2
				b. Contact window that has less than 40% of its perimeter covered by metallization.	Open	2	2
				c. A metallization path not intended to cover a contact window that is separated from the window by leaa than 0.1 mil.	Short Or Leakage	2	4
				d. Any exposure of the gate oxide bridge from source to drain diffusiona (applicable to MOS atructures).	Breakdown	4	3
				e. Any exposure of the gate oxide bridge that leaves leaa than 75% of the metallization coincident with the source and drain diffusion junction line undisturbed (applicable to MOS structures).	Breakdown	4	3

Table 4. (cont)

a. 2010.4 Para. No.	b. Defect Category	c. Magfn.	d. Altern.	e. Rejection Criteria	f. Potential Failure Mode	g. Difficulty	h. Criticality
3.2.1.7	Metallization Alignment (continued)	High	Delete	f. Gate metallization not coincident with or extending over the diffused guard ring.	Breakdown	4	3
3.2.2	Diffusion and Passivation Layer Faults	High	Delete	a. A diffusion junction line that unintentionally crosses another diffusion junction line.	Leakage Or Short	3	4
				b. Any isolation diffusion that is discontinuous (except isolation walls around unused areas or bonding pads) or any other diffused area with less than 25% of the original diffusion width remaining.	Undefined	3	2
				c. Either multiple lines or a complete absence of passivation visible at the edge and continuing under the metallization.	Leakage Or Short	4	3
				d. An active junction not covered by passivation, unless by design.	Leakage	3	3
3.2.3	Scribing and Die Defects	High	Low	a. Less than 0.1 mil of passivation visible between operating metallization or bond periphery and edge of the die.	Leakage	2	2
				b. Chipout in active circuit area.	Open	2	4
				c. Any substrate or passivation crack in the active circuit ares or a crack that exceeds 5.0 mils in length.	Open	3	4
				d. Any crack that comes closer than 0.1 mil to any operating metallization or other active circuit area on the die.	Open	3	3
				e. A crack, that exceeds 1.0 mil in length, inside the scribe grid or scribe line that points toward operating metallization or functional circuit elements.	Open	3	3
				f. Exposed silicon extending beyond the passivation edge at the point of the beam lead exit from the die (applicable to beam lead structures).	Open Or High Res.	2	2
				g. A crack that comes closer than 0.5 mil to operating beam lead metallization.	Open	3	3
3.2.4	Bond Defects:						
3.2.4.1	Gold Ball Bonds	Low	No Chg.	a. Gold ball bonds on the die or package post where the ball bond diameter is less than 2.0 times or greater than 6.0 times the wire diameter.	Open	2	2
				b. Gold ball bonds where the wire exit is not completely within the periphery of the ball.	Open	2	2

Table 4. (cont)

a. 2010.4 Para. No.	b. Defect Category	c. Magfn.	d. Altern.	e. Rejection Criteria	f. Potential Failure Mode	g. Difficulty	h. Criticality
3.2.4.1	Gold Ball Bonds (continued)			c. Gold ball bonds where the wire center exit is not within the boundaries of the bonding pad.	Open Or Leakage	2	2
				d. Intermetallic formation extending radially more than 0.1 mil completely around the periphery of any gold ball for that portion of the gold ball bond located on metal.	Leakage	2	3
3.2.4.2	Wedge Bonds	Low	No Chg.	a. Ultrasonic wedge bonds on the die or package post that are less than 1.2 times or greater than 3.0 times the wire diameter in width, or are less than 1.5 times or greater than 5.0 times the wire diameter in length.	Open	2	2
				b. Thermocompression wedge bonds on the die or package post that are less than 1.5 times or grester than 3.0 times the wire diameter in width, or sre less than 1.5 times or greater than 5.0 times the wire diameter in length.	Open	2	2
				c. Wedge bonds at the point where metallization exists from the bonding pad that do not exhibit a line of undisturbed metal visible between the periphery of the bond snd at least one side of the entering metallization stripe.	Open	3	2
3.2.4.3	Tailless Bonds	Low	No Chg.	a. Tailless bonds on the die or package post that are less than 1.2 times greater than 5.0 times the wire diameter in width, or are less than 0.5 times or greater than 3.0 times the wire diameter in length.	Open	2	2
				b. Tailless bonds where the bond impression does not cover entire width of the wire.	Open	2	2
				c. Tailless bonds at the point where metallization exits from the bonding pad that do not exhibit a line of undisturbed metal visible between the periphery of the bond and at least one side of the entering metallization stripe.	Open	3	2
3.2.4.4	General (Gold Ball Wedge and Tailless)	Low	No Chg.	a. Bonds on the die where less than 50% of the bond is within the unglassivated bonding pad area.	Open Or Leakage	2	2
				b. Bonds on the package post that are not completely within two package post widths from the inner edge of the package post.	Open	2	2
				c. Bonds placed so that the wire exiting from the bond crosses over another bond.	Short	1	3

Table 4. (cont)

a. 2010.4 Para. No.	b. Defect Category	c. Magfn.	d. Altern.	e. Rejection Criteria	f. Potential Failure Mode	g. Difficulty	h. Criticality
3.2.4.4	General (Gold Ball Wedge and Tailless) (continued).			d. Bonds placed so that the separation between bonds or the bond and operating metallization not connected to it is less than 0.1 mil.	Short	1	4
				e. Wire bond tails that extend over or make contact with any metallization not covered by glassivation and not connected to the wire.	Short	1	4
				f. Wire bond tails that exceed two wire diameters in length at the bonding pad or four wire diameters in length at the package post.	Short	2	2
				g. Bonds where less than 50% of the bond is located within an area that is free of die preform mounting material.	Open	2	2
				h. A bond on top of another bond, bond wire tail or residual segment of lead wire. An ultrasonic wedge bond alongside a previous bond where the obaervable width of the first bond is reduced less than 0.25 mils, is considered acceptable).	Open	1	2
				i. Any evidence of repair of conductors by bridging with or addition of bonding wire or ribbon.	Open	1	2
				j. Any rebonding which violates the applicable rework limitations of MIL-M-38510.	Open Or Short	1	N
3.2.4.5	Beam Lead. (Criteria Applies to the Completed Bond Area).	Low	No Chg.	a. Bonds where the tool impression does not completely cross the entire beam width.	Open	2	3
				b. Bonds on thin film substrate metal where the tool impression increases the beam lead width less than 15% (10% for compliant bonds) or greater than 75% of the undeformed beam width.	Open	3	3
				c. Bonds where the tool impression length is less than 1.0 mil.	Open	2	3
				d. A bonding tool impression less than 1.0 mil from the die edge.	Open	2	2
				e. Effective bonded area less than 50% of that which would be possible for an exactly aligned beam.	Open	2	2
				f. Cracks or tears in the effective bonded area of the beam greater than 50% of the original beam width.	Open	2	3
				g. Bonds placed so that the separation between bonds or between bonds and operating metallization not connected to them is less than 0.1 mil.	Short	1	4

Table 4. (cont)

a. 2010.4 Para. No.	b. Defect Category	c. Magfn.	d. Altern.	e. Rejection Criteria	f. Potential Failure Mode	g. Difficulty	h. Criticality
3.2.4.5	Beam Lead. (Criteria Applies to the Completed Bond Area). (continued)			h. Bonds lifting or peeling.	Open	1	4
3.2.5	Internal Leads:						
3.2.5.1	Wires	Low	No Chg.	a. Any wire that touches another wire (excluding common wires), package post, unglassivated operating metallization, die, or any portion of the package.	Short	1	4
				b. Excessive loop or sag in any wire so that it comes closer than two wire diameters to another wire, package post, unglassivated operating metallization or die, or portion of the package after a spherical radial distance from the bond perimeter on the die surface of 5.0 mils for ball bonds, or 10 mils for ultrasonic and thermocompreasion bonds.	Short	1	1
				c. Nicka, cuts, crimpa, scoring, or neckdown in any wire that reduces the wire diameter by more than 25%.	Open	2	2
				d. Attached extra wire greater than two wire diametera in length at the bonding pad or four wire diametera in length at the package post.	Short	1	1
				e. Tearing at the junction of the wire and bond.	Open	1	3
				f. Any wire making a straight line run from die bonding pad to package post that has no arc.	Open	1	2
				g. Wire(s) crossing wire(s) (except common conductors)	Short	1	4
				h. Wire(s) not in accordance with bonding diagram.	Any	2	4
3.2.5.2	Beams	Low	No Chg.	a. Voids, nicks, depressions, or acratchea that leave leas than 50% of the heam width undisturbed.	Open	2	3
				b. Beam separation from the die.	Open	1	4
				c. Missing or partially fabricated beam leads, unlesa by deaign.	Open	1	4
				d. Beam leads that are not bonded.	Open	1	4
				e. Bonded area closer than 0.1 mil to the edge of the passivation layer.	Leakage	2	3
				f. Lack of evidence of a paaaivation layer between the die and each beam.	Leakage	2	3

Table 4. (cont)

a. 2010.4 Para. No.	b. Defect Category	c. Magfn.	d. Altern.	e. Rejection Criteria	f. Potential Failure Mode	g. Difficulty	h. Criticality
3.2.6	Package Conditions:						
3.2.6.1	Foreign Material	Low	No Chg.	a. Unattached foreign material on the surface of the die or within the package.	Leakage Or Short	1	1
				b. Unattached foreign material on the surface of the lid or cap.	Contamination	1	1
				c. Attached conductive foreign material that bridges metallization paths, package leads, lead to package metalization, functional circuit elements or junctions, or any combination thereof.	Short	2	4
				d. Ink on the surface of the die that covers more than 25% of a bonding pad area or that bridges any combination of unglassivated metallization or bare silicon areas.	Leakage	2	1
3.2.6.2	Die Mounting	Low	No Chg.	a. Die mounting material buildup that extends onto the top surface of the die.	Leakage	1	1
				b. Die to header mounting material not visible around at least 50% of the die perimeter unless it is continuous on two full nonadjacent sides of the die, except for transparent die.	Undefined	1	1
				c. Transparent die with less than 50% of the area bonded.	Undefined	2	1
				d. Flaking of the die mounting material.	Leakage	1	2
				e. Balling of the die mounting material that does not exhibit a fillet. when viewed from above.	Undefined	1	1
3.2.6.3	Die Assembly	Low	No Chg.	a. Die not located and oriented in accordance with applicable assembly drawing of the device.	Undefined	1	4
3.2.7	Glassivation Defects:	High	Delete	a. Crazing that prohibits the detection of visual criteria contained herein.	Undefined	1	N
				b. Any lifting or pulling of the glassivation.	Leakage	1	2
				c. Two or more adjacent active metallization paths not covered by glassivation, excluding bonding pad cutouts.	Leakage	1	2
				d. Unglassivation areas greater than 5.0 mils in any dimension, unless by design.	Undefined	1	2
				e. Unglassivation areas at the edge of bonding pad exposing silicon.	Leakage	2	2

Table 4. (cont)

a. 2010.4 Para. No.	b. Defect Category	c. Magfn.	d. Altern.	e. Rejection Criteria	f. Potential Failure Mode	g. Difficulty	h. Criticality
3.2.7	Glaasivation Defects: (continued)	High	Delete	f. Glaasivation covering more than 50% of the bonding pad area.	Open	1	2
				g. Crazing over a film resistor.	Undefined	2	1
3.2.8	Dielectric Isolation Defecta	High	Delete	a. A discontinuoua isolation line (typically a black line) around each diffusion tub containing functional circuit elements.	Undefined	3	1
				b. Absence of a continuous isolation line between any adjacent tubs containing functional circuit elementa.	Leakage	3	1
				c. A diffused area which overlapa dielectric iaolation material and comea closer than 0.1 mil to an adjacent diffusion tub; or an overlap of more than one diffuaion area into the dielectric isolation material.	Leakage Or Short	4	3
				d. A contact window that touches or overlaps dielectric isolation material.	Leakage	2	3
				e. Metallization acratch and void defecta over a dielectric isolation atep shall be in accordance with criteria in 3.2.1.1 b and 3.2.1.2 b.	-	-	
3.2.9	Film Resistor Defects	High	Delete	Metallization defect criteria of 3.2.1 shall apply.			
				a. Any misalignment between the conductor/resistor in which the actual width χ of the overlap ia leaa than 50% of the original resistor width.	R Change	3	2
				b. Contact overlap between the mteallization and film reaiator in which the length dimension Y is less than 0.25 mil.	Open	4	2
				c. Separation between any two resistora or a reaistor and a metallization path that ia lesa than 0.1 mil, unless by design.	Short	4	4
				d. Void or necking down that leaves leas than 75% of the film resistor width undiaturbed at a terminal.	R Change	3	2
				e. Any aharp change in the color of reaistor material, within 0.1 mil of the resistor/conductor termination.	R Change	3	2
				f. Inactive resistor inadvertently connected to two aeparate points of an active circuit.	Undefined	3	4
				g. Any thin film resistor that croases a aubstrate irregularity (e.g., dielectric iaolation line, oxide/diffuaion atep, etc.),	Undefined	3	2

Table 4. (cont)

COLUMN	DESCRIPTION
a.	Paragraph number from METHOD 2010.4, MIL-STD-883B that defines the inspection requirement and reject criteria.
b.	Category of defect.
c.	Magnification level required for each inspection (Class B): "High" is 75X to 100X, "Low" is 30X to 60X.
d.	Alternate screening devistions for complex microcircuits when requirements of METHOD 5004 "alternate procedures" are employed.
e.	Rejection criteria to be imposed during the internal visual screening inspection.
f.	Potential failure mode given that a failure developed as a result of overlooked defect.
g.	Difficulty - estimate of relative level of concentration and discipline necessary to perform flawless inspection for each criteria related defect. (1 = least, 4 = most).
h.	Criticality - estimated chance that device failure occurs if the criteria related defects are not screened out. (1 = least, 4 = most).

Table 5. Integrated circuit inspection microscope systems

MANUFACTURER	MODEL	MAGNIFICATION		LIGHTING			VIDEO COMPATIBILITY	SPECIAL FEATURES
		30X-60X	75X-150X	BRIGHTFIELD	BRIGHTFIELD/ DARKFIELD	NOMARSKI		
Bauach & Lomb	Microfilm ZMT2A	50.63X w/amplifier	120X	✓	✓	-	✓	• In-focus zoom attachment • "Lazy Susan" 4 wafer paddle
Olympua	BHMJL	50X	100X	✓	✓	✓	-	• Y-direction lock for accurate X-axis acan.
Nikon	IC Inspection Microscopes	50X	100X	✓	✓	✓	-	• CF optics, aliminates chromatic abberations.
American Optical	AO Series 1860	65X	100X	✓	✓	✓	-	• Nosepiece movement focuaing • Variable auto focua stop, prevents contact w/IC.
Vickers	M45	40X	100X	✓	✓	-	✓	• Brightfield/Darkfield sliding control.
Vision Engineering	VJ5	30X-60X	75X-100X	✓	-	-	N/a	• Dynascopic projection • Continuously variable zoom, 5X to 100X.
Applied Materials	CI-750	50X	100X	✓	✓	✓	-	• Automatic input belts, positioning, and output indexers. • Sorting data storage.
Adcotech	Series 3000-I	?	?	✓	-	-	✓	• Automatic input tubes and output indexers • Sorting data readout.
Operations Technology	OPTEK 101	50X	-	✓	-	-	N/a	• Viewing screen. • Motorized X-Y table.
Metron	3-D Hybrid Comparator	30X	-	✓	-	-	N/a	• 3-D comparison with "master" IC.

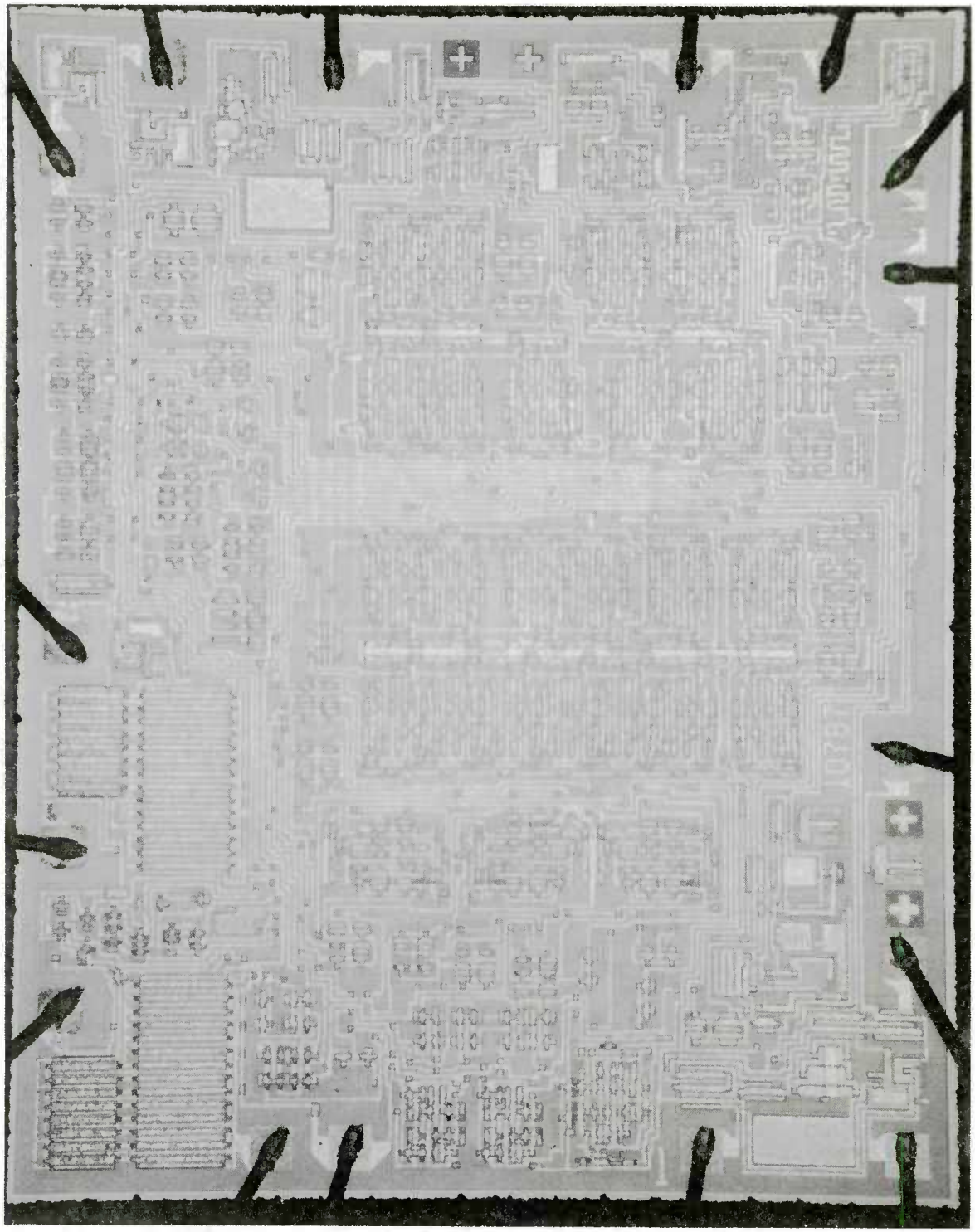

Figure 1. RCA timer chip

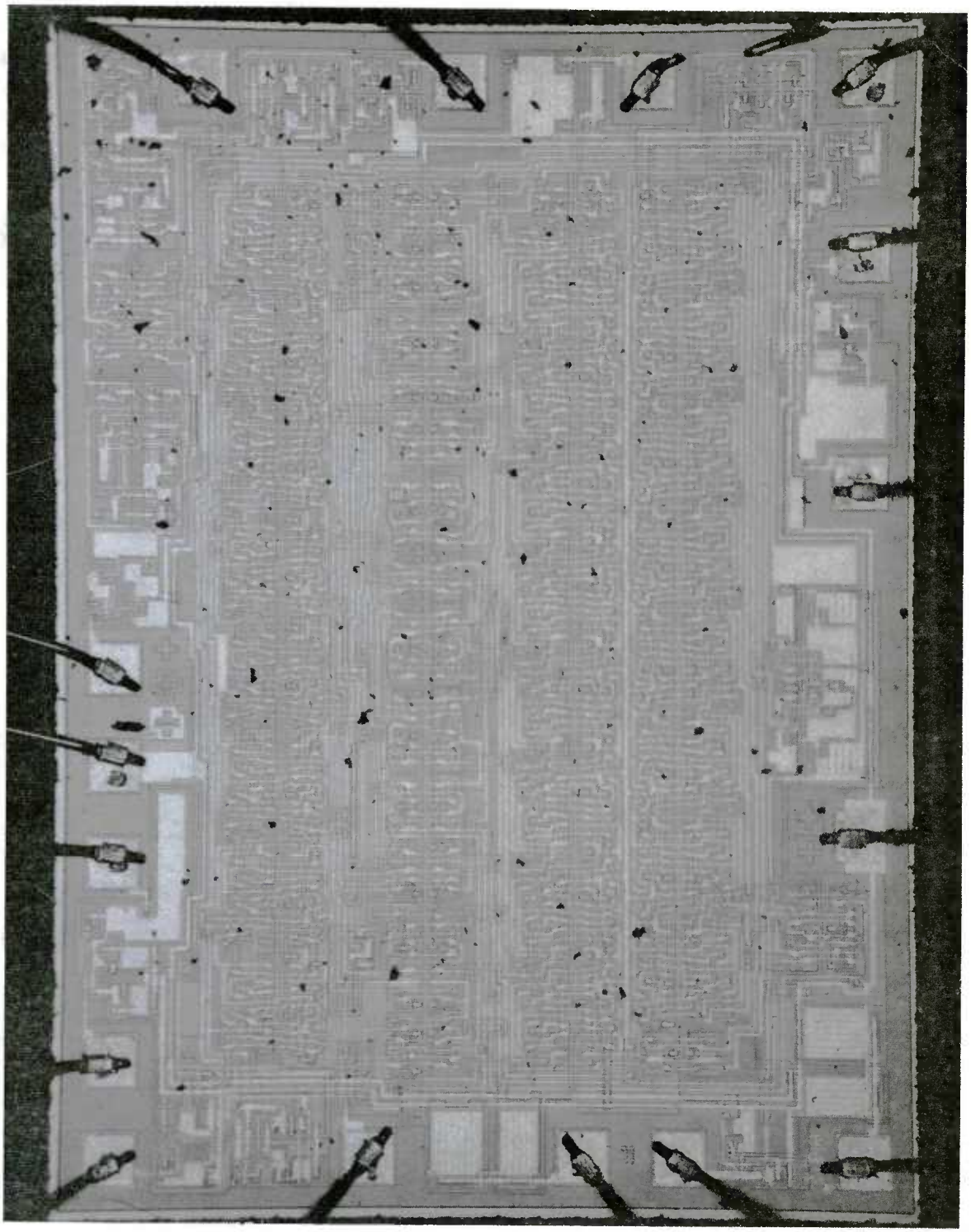

Figure 2. Motorola timer chip

APPENDIX

SCOPE OF WORK

F. 1. SCOPE OF WORK

I. Objective

The contractor shall devote his technical knowledge, engineering and scientific expertise in the investigation of implementing an automatic inspection system that performs the Internal Visual Inspection of MIL-STD-883 Test Method 2010. The inspection system will be used on integrated circuit (IC) packages incorporated in the FASCAM programs and have the capability of being adaptable to future programs. The following objectives for this phase of the program shall be met.

A. The frequency of occurrence of each of the defects found in MIL-STD-883, Test Method 2010, should be determined.

B. The consequence of each defect should be investigated with respect to safety and reliability in the FASCAM programs.

C. The degree of difficulty anticipated in detecting individual defects utilizing an automatic inspection system shall be estimated.

D. Alternative methods of inspecting the defects should be investigated.

E. Current techniques presently being used in the field relating to this type of inspection should be investigated whether automated or manual/visual.

F. Provide cost parameters anticipated for an automatic inspection system.

II. Background

The Family of Scatterable Mines (FASCAM) utilizes Large Scale Integrated Circuits (LSIC) in their electronic fuzes. Defects in the LSIC's can affect both the safe-separation and the self-sterlization features of FASCAM. Therefore, 100% pre-cap visual inspection, per MIL-STD-883, Test Methods and Procedures for micro-electronics, is required to prevent safety-related defects (criticals). The inspection is costly, labor intensive, and is not available from all semi-conductor manufacturers.

III. Procedure

A. At the earliest possible time, but not later than 30 December 1981, the contractor shall submit the results of his investigation.

B. The submission (written report) shall discuss the methods of analysis used to obtain the reported information.

IV. Requirements

A. The objectives should be investigated using the timer chip, Drawing Nos. 9287165/6, as the basic I.C. for this program.

B. MIL-STD-883 Test Method 2010 shall be the documentation used to meet objectives.

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